



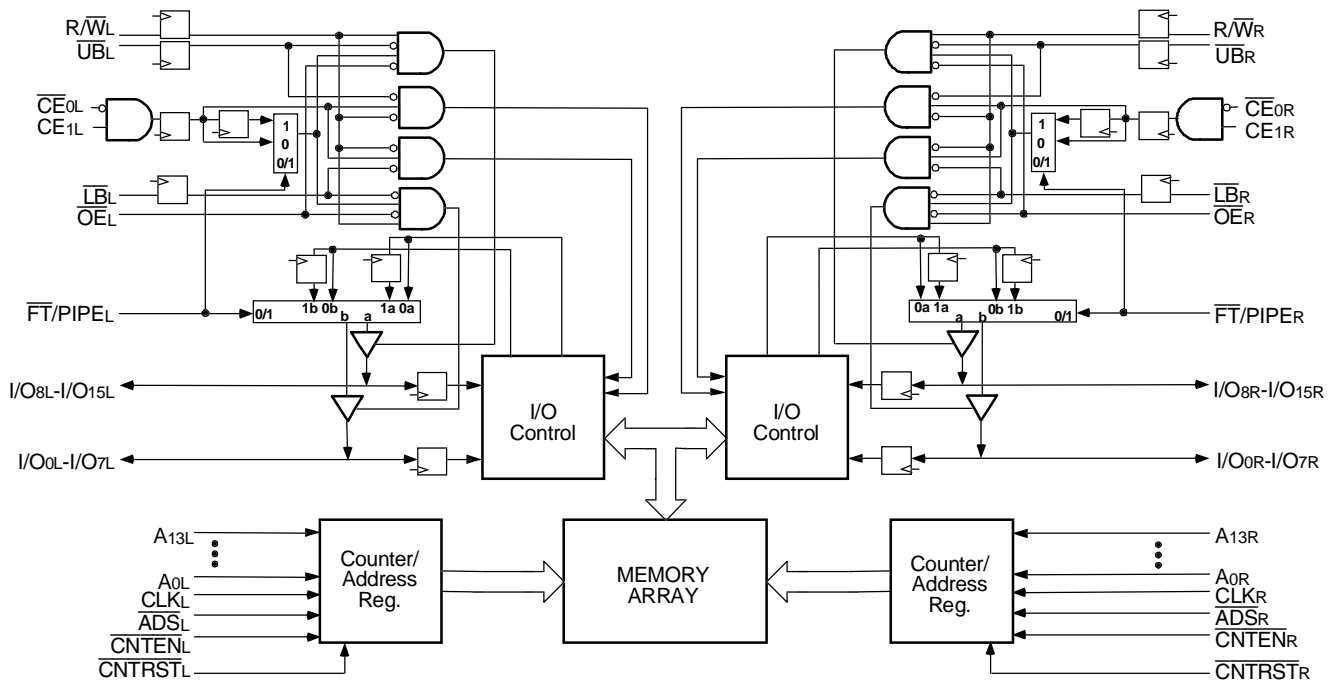
HIGH-SPEED 16K x 16 SYNCHRONOUS PIPELINED DUAL-PORT STATIC RAM

**PRELIMINARY
IDT709269S/L**

Features:

- ◆ True Dual-Ported memory cells which allow simultaneous access of the same memory location
 - ◆ High-speed clock to data access
 - Commercial: 9/12/15ns (max.)
 - ◆ Low-power operation
 - IDT709269S
Active: 950mW (typ.)
Standby: 5mW (typ.)
 - IDT709269L
Active: 950mW (typ.)
Standby: 1mW (typ.)
 - ◆ Flow-through or Pipelined output mode on either port via the FT/PIPE pin
 - ◆ Counter enable and reset features
 - ◆ Dual chip enables allow for depth expansion without additional logic
- ◆ Full synchronous operation on both ports
 - 4ns setup to clock and 1ns hold on all control, data, and address inputs
 - Data input, address, and control registers
 - Fast 9ns clock to data out in the Pipelined output mode
 - Self-timed write allows fast cycle time
 - 15ns cycle time, 66MHz operation in Pipelined output mode
 - ◆ Separate upper-byte and lower-byte controls for multiplexed bus and bus matching compatibility
 - ◆ TTL-compatible, single 5V (±10%) power supply
 - ◆ Industrial temperature range (-40°C to +85°C) is available for selected speeds
 - ◆ Available in a 100-pin Thin Quad Flatpack (TQFP) package

Functional Block Diagram



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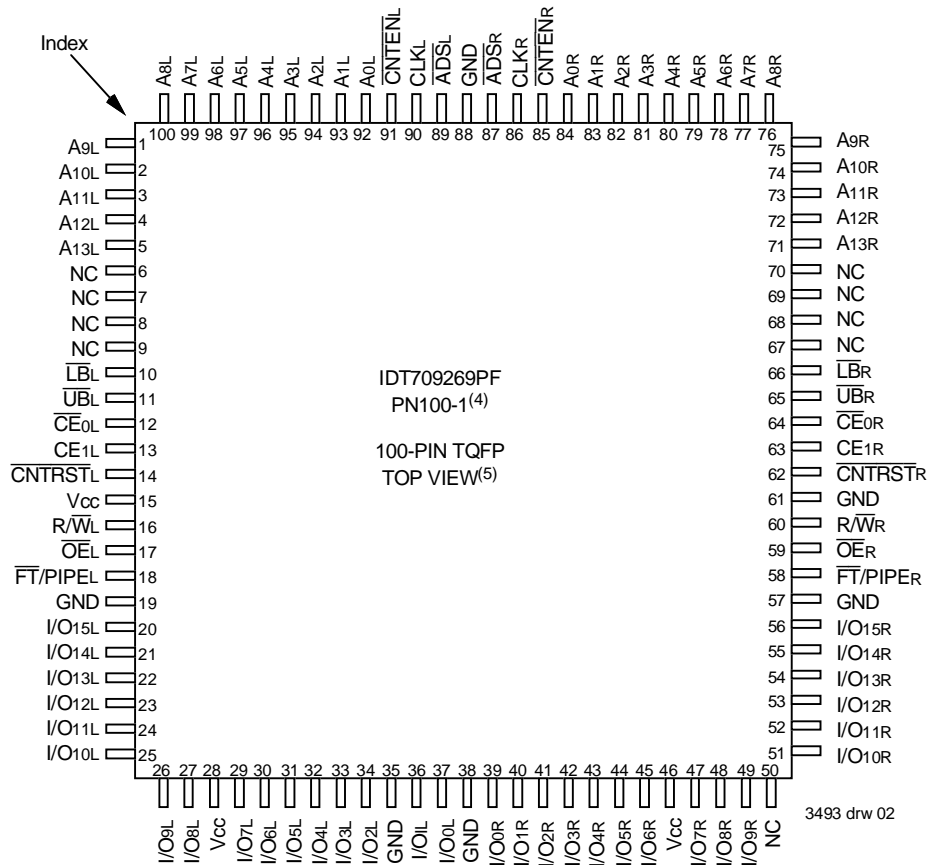
APRIL 2000

Description:

The IDT709269 is a high-speed 16K x 16 bit synchronous pipelined Dual-Port RAM. The memory array utilizes Dual-Port memory cells to allow simultaneous access of any address from both ports. Registers on control, data, and address inputs provide minimal setup and hold times. The timing latitude provided by this approach allows systems to be designed with very short cycle times.

With an input data register, the IDT709269 has been optimized for applications having unidirectional or bidirectional data flow in bursts. An automatic power down feature, controlled by \overline{CE}_0 and CE_1 , permits the on-chip circuitry of each port to enter a very low standby power mode. Fabricated using IDT's CMOS high-performance technology, these devices typically operate on only 950mW of power.

Pin Configuration^(1,2,3)



NOTES:

1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground supply.
3. Package body is approximately 14mm x 14mm x 1.4mm
4. This package code is used to reference the package diagram.
5. This text does not indicate orientation of the actual part-marking.

Pin Names

Left Port	Right Port	Names
\overline{CE}_{0L} , CE1L	\overline{CE}_{0R} , CE1R	Chip Enables
R/ \overline{WL}	R/ \overline{WR}	Read/Write Enable
\overline{OE}_L	\overline{OE}_R	Output Enable
A0L - A13L	A0R - A13R	Address
I/O0L - I/O15L	I/O0R - I/O15R	Data Input/Output
CLKL	CLKR	Clock
\overline{UB}_L	\overline{UB}_R	Upper Byte Select
\overline{LB}_L	\overline{LB}_R	Lower Byte Select
\overline{ADS}_L	\overline{ADS}_R	Address Strobe
\overline{CNTEN}_L	\overline{CNTEN}_R	Counter Enable
\overline{CNTRST}_L	\overline{CNTRST}_R	Counter Reset
$\overline{FT/PIPE}_L$	$\overline{FT/PIPE}_R$	Flow-Through/Pipeline
Vcc		Power
GND		Ground

3493 tbl 01

Truth Table I—Read/Write and Enable Control^(1,2,3)

\overline{OE}	CLK	\overline{CE}_0	CE1	\overline{UB}	\overline{LB}	R \overline{W}	Upper Byte I/O8-15	Lower Byte I/O0-7	Mode
X	↑	H	X	X	X	X	High-Z	High-Z	Deselected—Power Down
X	↑	X	L	X	X	X	High-Z	High-Z	Deselected—Power Down
X	↑	L	H	H	H	X	High-Z	High-Z	Both Bytes Deselected
X	↑	L	H	L	H	L	D _{IN}	High-Z	Write to Upper Byte Only
X	↑	L	H	H	L	L	High-Z	D _{IN}	Write to Lower Byte Only
X	↑	L	H	L	L	L	D _{IN}	D _{IN}	Write to Both Bytes
L	↑	L	H	L	H	H	D _{OUT}	High-Z	Read Upper Byte Only
L	↑	L	H	H	L	H	High-Z	D _{OUT}	Read Lower Byte Only
L	↑	L	H	L	L	H	D _{OUT}	D _{OUT}	Read Both Bytes
H	X	L	H	L	L	X	High-Z	High-Z	Outputs Disabled

NOTES:

- "H" = V_{IH}, "L" = V_{IL}, "X" = Don't Care.
- \overline{ADS} , \overline{CNTEN} , \overline{CNTRST} = X.
- \overline{OE} is an asynchronous input signal.

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TRUTH TABLE II—Address Counter Control^(1,2)

Address	Previous Address	CLK	\overline{ADS}	\overline{CNTEN}	\overline{CNRST}	I/O ⁽³⁾	Mode
X	X	↑	H	H	L	D _{IO(0)}	Counter Reset to Address 0
An	X	↑	L ⁽⁴⁾	H	H	D _{IO(n)}	External Address Utilized
X	An	↑	H	H	H	D _{IO(n)}	External Address Blocked—Counter Disabled
X	An	↑	H	L ⁽⁵⁾	H	D _{IO(n+1)}	Counter Enable—Internal Address Generation

3493 tbl 03

NOTES:

- "H" = V_{IH}, "L" = V_{IL}, "X" = Don't Care.
- $\overline{CE0}$, \overline{LB} , \overline{UB} , and \overline{OE} = V_{IL}; CE₁ and R/ \overline{W} = V_{IH}.
- Outputs configured in Flow-Through Output mode; if outputs are in Pipelined mode the data out will be delayed by one cycle.
- \overline{ADS} is independent of all other signals including $\overline{CE0}$, CE₁, \overline{UB} and \overline{LB} .
- The address counter advances if \overline{CNTEN} = V_{IL} on the rising edge of CLK, regardless of all other signals including $\overline{CE0}$, CE₁, \overline{UB} and \overline{LB} .

Recommended Operating Temperature and Supply Voltage^(1,2)

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%
Industrial	-40°C to +85°C	0V	5.0V ± 10%

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NOTES:

- This is the parameter T_A.
- Industrial temperature: for specific speeds, packages and powers contact your sales office.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V _{IH}	Input High Voltage	2.2	—	6.0 ⁽¹⁾	V
V _{IL}	Input Low Voltage	-0.5 ⁽²⁾	—	0.8	V

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NOTES:

- V_{TERM} must not exceed Vcc + 10%.
- V_{IL} ≥ -1.5V for pulse width less than 10ns.

Absolute Maximum Ratings⁽¹⁾

Symbol	Rating	Commercial & Industrial	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T _{BIAS}	Temperature Under Bias	-55 to +125	°C
T _{STG}	Storage Temperature	-55 to +125	°C
I _{OUT}	DC Output Current	50	mA

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NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{TERM} must not exceed Vcc + 10% for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of V_{TERM} ≥ Vcc + 10%.

Capacitance (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions ⁽²⁾	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 3dV	9	pF
C _{OUT} ⁽³⁾	Output Capacitance	V _{OUT} = 3dV	10	pF

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NOTES:

- These parameters are determined by device characterization, but are not production tested.
- 3dV references the interpolated capacitance when the input and output switch from 0V to 3V or from 3V to 0V.
- C_{OUT} also references C_{I/O}.

DC Electrical Characteristics Over the Operating Temperature Supply Voltage Range ($V_{CC} = 5.0V \pm 10\%$)

Symbol	Parameter	Test Conditions	709269S/L		Unit
			Min.	Max.	
$ I_{II} $	Input Leakage Current ⁽¹⁾	$V_{CC} = 5.5V, V_{IN} = 0V \text{ to } V_{CC}$	—	10	μA
$ I_{LO} $	Output Leakage Current	$\overline{CE}_0 = V_{IH} \text{ or } CE_1 = V_{IL}, V_{OUT} = 0V \text{ to } V_{CC}$	—	10	μA
V_{OL}	Output Low Voltage	$I_{OL} = +4mA$	—	0.4	V
V_{OH}	Output High Voltage	$I_{OH} = -4mA$	2.4	—	V

NOTE:

- At $V_{CC} \leq 2.0V$ input leakages are undefined.

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DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range^(6,7) ($V_{CC} = 5V \pm 10\%$)

Symbol	Parameter	Test Condition	Version	709269X9 Com'l Only		709269X12 Com'l Only		709269X15 Com'l Only		Unit	
				Typ. ⁽⁴⁾	Max.	Typ. ⁽⁴⁾	Max.	Typ. ⁽⁴⁾	Max.		
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}_L \text{ and } \overline{CE}_R = V_{IL}$ Outputs Open $f = f_{MAX}^{(1)}$	COM'L	S	210	390	200	345	190	325	mA
				L	210	350	200	305	190	285	
ISB1	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L = \overline{CE}_R = V_{IH}$ $f = f_{MAX}^{(1)}$	COM'L	S	50	135	50	110	50	110	mA
				L	50	115	50	90	50	90	
ISB2	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_A^* = V_{IL}$ and $\overline{CE}_B^* = V_{IH}^{(3)}$ Active Port Outputs Open, $f = f_{MAX}^{(3)}$	COM'L	S	140	270	130	230	120	220	mA
				L	140	240	130	200	120	190	
ISB3	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports \overline{CE}_R and $\overline{CE}_L \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V, f = 0^{(2)}$	COM'L	S	1.0	15	1.0	15	1.0	15	mA
				L	0.2	5	0.2	5	0.2	5	
ISB4	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}_A^* \leq 0.2V$ and $\overline{CE}_B^* \geq V_{CC} - 0.2V^{(6)}$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V, \text{ Active Port Outputs Open, } f = f_{MAX}^{(1)}$	COM'L	S	130	245	120	205	110	195	mA
				L	130	225	120	185	110	175	
			IND	S	—	—	—	—	—	—	
				L	—	—	—	—	—	—	

NOTES:

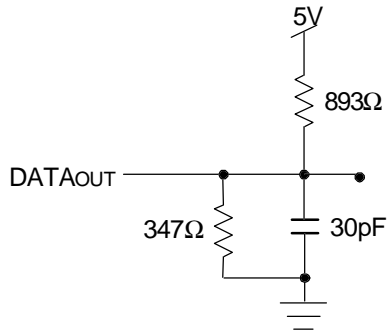
- At $f = f_{MAX}$, address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of $1/t_{cyc}$, using "AC TEST CONDITIONS" at input levels of GND to 3V.
- $f = 0$ means no address, clock, or control lines change. Applies only to input at CMOS level standby.
- Port "A" may be either left or right port. Port "B" is the opposite from port "A".
- $V_{CC} = 5V, T_A = 25^\circ C$ for Typ, and are not production tested. $I_{CC DC}(f=0) = 150mA$ (Typ).
- $\overline{CE}_X = V_{IL}$ means $\overline{CE}_{0X} = V_{IL}$ and $CE_{1X} = V_{IH}$
 $\overline{CE}_X = V_{IH}$ means $\overline{CE}_{0X} = V_{IH}$ or $CE_{1X} = V_{IL}$
 $\overline{CE}_X \leq 0.2V$ means $\overline{CE}_{0X} \leq 0.2V$ and $CE_{1X} \geq V_{CC} - 0.2V$
 $\overline{CE}_X \geq V_{CC} - 0.2V$ means $\overline{CE}_{0X} \geq V_{CC} - 0.2V$ or $CE_{1X} \leq 0.2V$
 "X" represents "L" for left port or "R" for right port.
- 'X' in part number indicates power rating (S or L).
- Industrial temperature: for specific speeds, packages and powers contact your sales office.

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AC Test Conditions

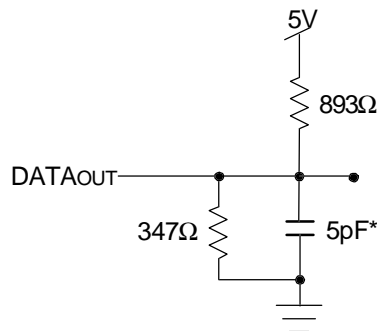
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1,2 and 3

3493 tbl 10



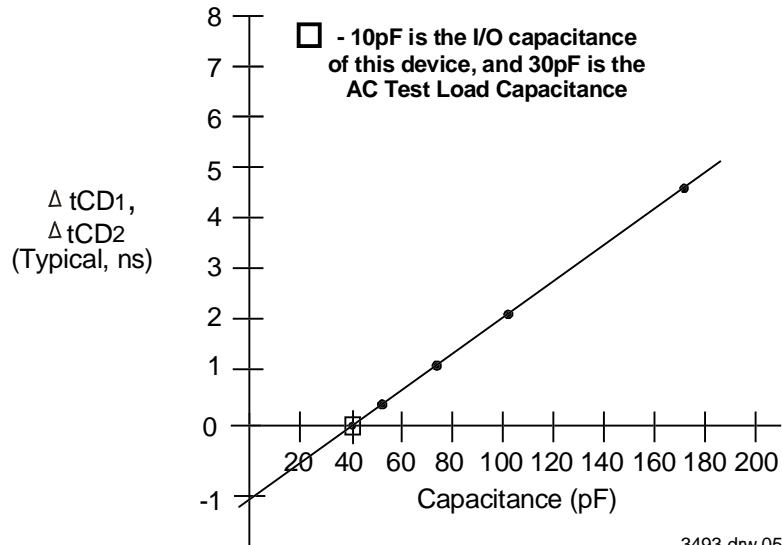
3493 drw 03

Figure 1. AC Output Test load.



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Figure 2. Output Test Load
(For t_{CKLZ}, t_{CKHZ}, t_{OLZ}, and t_{OHZ}).
*Including scope and jig.



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Figure 3. Typical Output Derating (Lumped Capacitive Load).

AC Electrical Characteristics Over the Operating Temperature Range (Read and Write Cycle Timing)^(3,4,5) ($V_{CC} = 5V \pm 10\%$, $T_A = 0^\circ C$ to $+70^\circ C$)

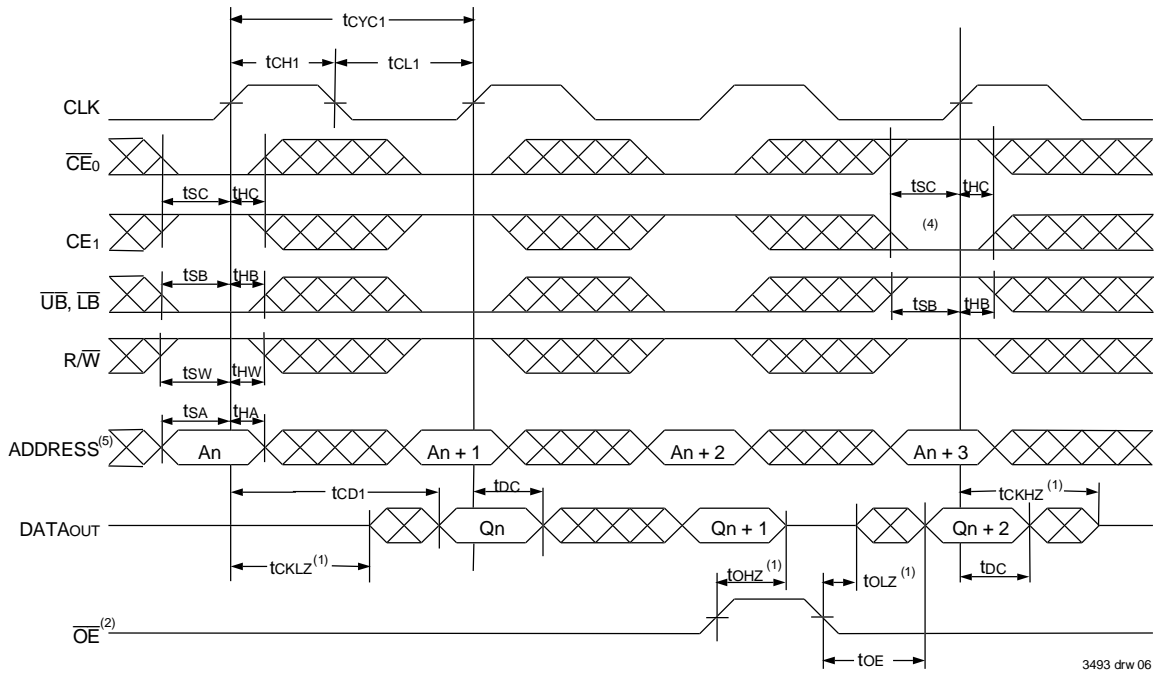
Symbol	Parameter	709269X9 Com'1 Only		709269X12 Com'1 Only		709269X15 Com'1 Only		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{CYC1}	Clock Cycle Time (Flow-Through) ⁽²⁾	25	—	30	—	35	—	ns
t _{CYC2}	Clock Cycle Time (Pipelined) ⁽²⁾	15	—	20	—	25	—	ns
t _{CH1}	Clock High Time (Flow-Through) ⁽²⁾	12	—	12	—	12	—	ns
t _{CL1}	Clock Low Time (Flow-Through) ⁽²⁾	12	—	12	—	12	—	ns
t _{CH2}	Clock High Time (Pipelined) ⁽²⁾	6	—	8	—	10	—	ns
t _{CL2}	Clock Low Time (Pipelined) ⁽²⁾	6	—	8	—	10	—	ns
t _r	Clock Rise Time	—	3	—	3	—	3	ns
t _f	Clock Fall Time	—	3	—	3	—	3	ns
t _{SA}	Address Setup Time	4	—	4	—	4	—	ns
t _{HA}	Address Hold Time	1	—	1	—	1	—	ns
t _{SC}	Chip Enable Setup Time	4	—	4	—	4	—	ns
t _{HC}	Chip Enable Hold Time	1	—	1	—	1	—	ns
t _{SB}	Byte Enable Setup Time	4	—	4	—	4	—	ns
t _{HB}	Byte Enable Hold Time	1	—	1	—	1	—	ns
t _{SW}	R/ \bar{W} Setup Time	4	—	4	—	4	—	ns
t _{HW}	R/ \bar{W} Hold Time	1	—	1	—	1	—	ns
t _{SD}	Input Data Setup Time	4	—	4	—	4	—	ns
t _{HD}	Input Data Hold Time	1	—	1	—	1	—	ns
t _{SAD}	\overline{ADS} Setup Time	4	—	4	—	4	—	ns
t _{HAD}	\overline{ADS} Hold Time	1	—	1	—	1	—	ns
t _{SCN}	\overline{CNTEN} Setup Time	4	—	4	—	4	—	ns
t _{HCN}	\overline{CNTEN} Hold Time	1	—	1	—	1	—	ns
t _{SRST}	\overline{CNTRST} Setup Time	4	—	4	—	4	—	ns
t _{HRST}	\overline{CNTRST} Hold Time	1	—	1	—	1	—	ns
t _{OE}	Output Enable to Data Valid	—	12	—	12	—	15	ns
t _{OLZ}	Output Enable to Output Low-Z ⁽¹⁾	2	—	2	—	2	—	ns
t _{OHZ}	Output Enable to Output High-Z ⁽¹⁾	1	7	1	7	1	7	ns
t _{CD1}	Clock to Data Valid (Flow-Through) ⁽²⁾	—	20	—	25	—	30	ns
t _{CD2}	Clock to Data Valid (Pipelined) ⁽²⁾	—	9	—	12	—	15	ns
t _{DC}	Data Output Hold After Clock High	2	—	2	—	2	—	ns
t _{CKHZ}	Clock High to Output High-Z ⁽¹⁾	2	9	2	9	2	9	ns
t _{CKLZ}	Clock High to Output Low-Z ⁽¹⁾	2	—	2	—	2	—	ns
Port-to-Port Delay								
t _{CWDD}	Write Port Clock High to Read Data Delay	—	40	—	40	—	50	ns
t _{CCS}	Clock-to-Clock Setup Time	—	15	—	15	—	20	ns

NOTES:

3493 tbl 11

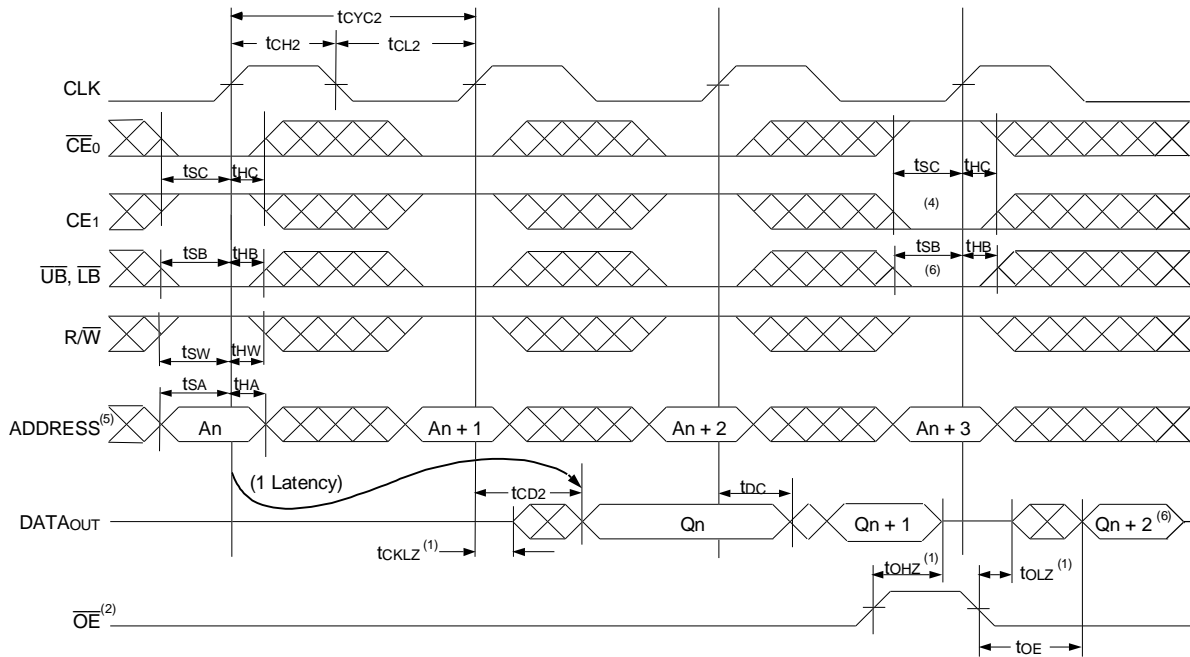
- Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2). This parameter is guaranteed by device characterization, but is not production tested.
- The Pipelined output parameters (t_{CYC2}, t_{CD2}) apply to either or both left and right ports when $\overline{FT}/PIPE = V_{IH}$. Flow-through parameters (t_{CYC1}, t_{CD1}) apply when $\overline{FT}/PIPE = V_{IL}$ for that port.
- All input signals are synchronous with respect to the clock except for the asynchronous Output Enable (\overline{OE}) and $\overline{FT}/PIPE$.
- 'X' in part number indicates power rating (S or L).
- Industrial temperature: for specific speeds, packages and powers contact your sales office.

Timing Waveform of Read Cycle for Flow-through Output on Either Port ($\overline{FT}/PIPEX = V_{IL}$)⁽³⁾



3493 drw 06

Timing Waveform of Read Cycle for Pipelined Operation on Either Port ($\overline{FT}/PIPEX = V_{IH}$)⁽³⁾

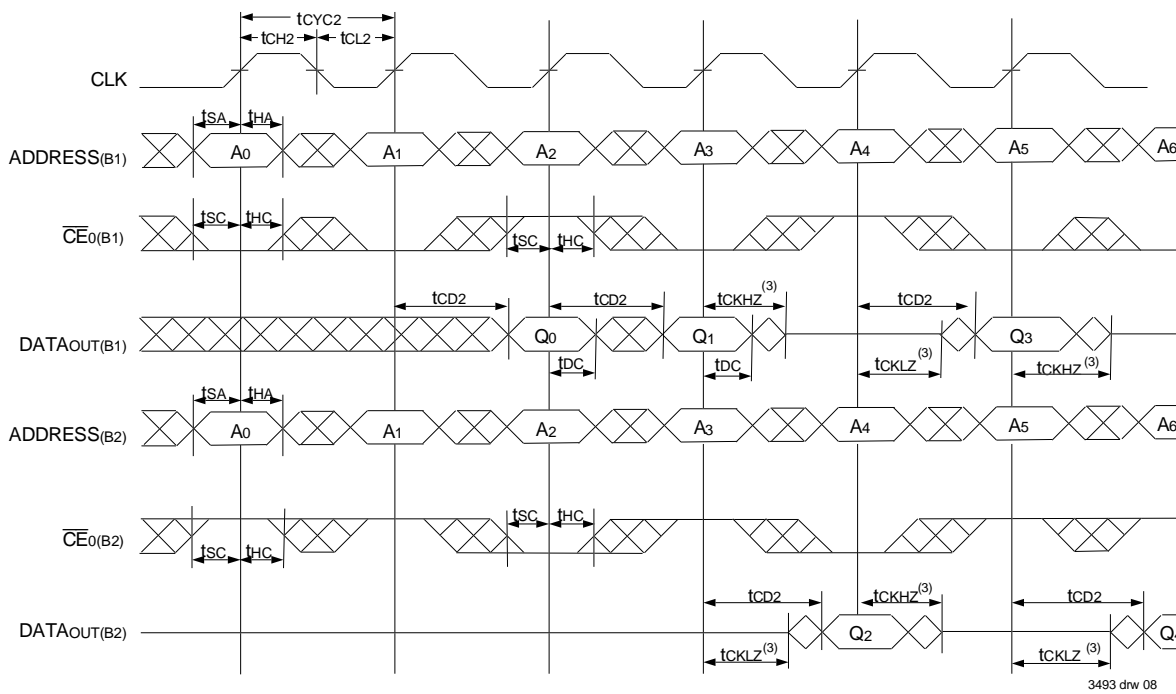


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NOTES:

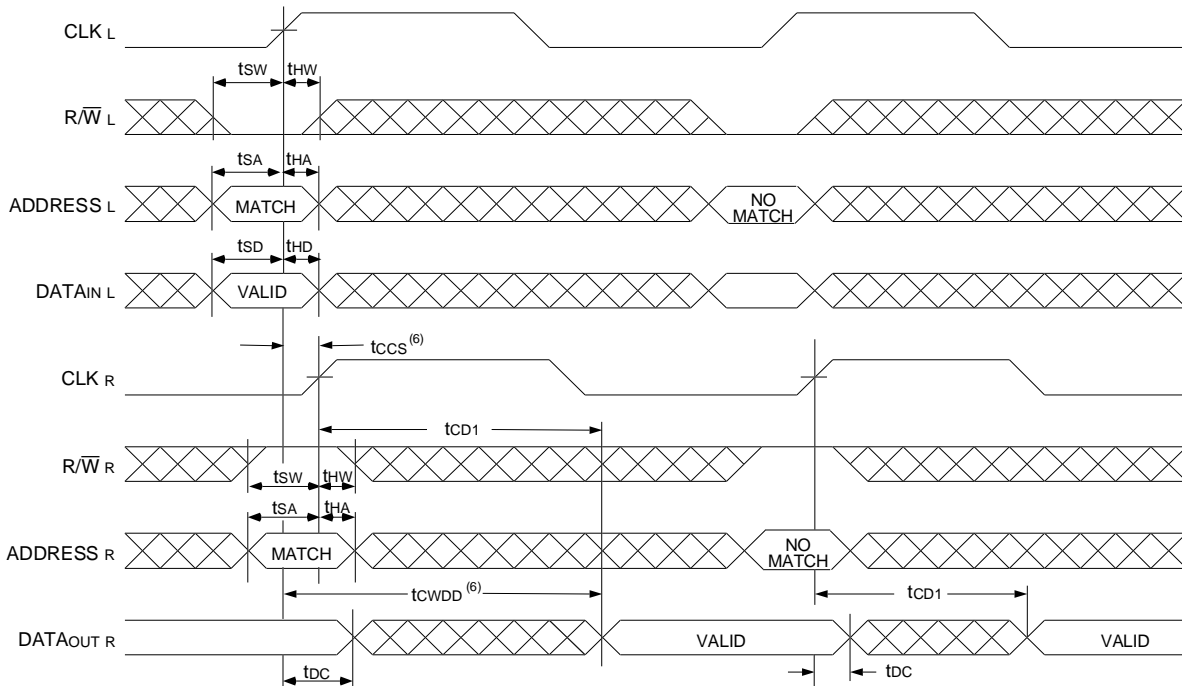
1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. \overline{OE} is asynchronously controlled; all other inputs are synchronous to the rising clock edge.
3. $\overline{ADS} = V_{IL}$, \overline{CNTEN} and $\overline{CNTRST} = V_{IH}$.
4. The output is disabled (High-impedance state) by $\overline{CE0} = V_{IH}$, $CE1 = V_{IL}$, $\overline{UB} = V_{IH}$, or $\overline{LB} = V_{IH}$ following the next rising edge of the clock. Refer to Truth Table 1.
5. Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
6. If \overline{UB} or \overline{LB} was HIGH, then the Upper Byte and/or Lower Byte of DATAout for $Qn + 2$ would be disabled (High-impedance state).

Timing Waveform of a Multi-device Pipelined Read^(1,2)



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Timing Waveform of Left Port Write to Flow-through Right Port Read^(4,5)

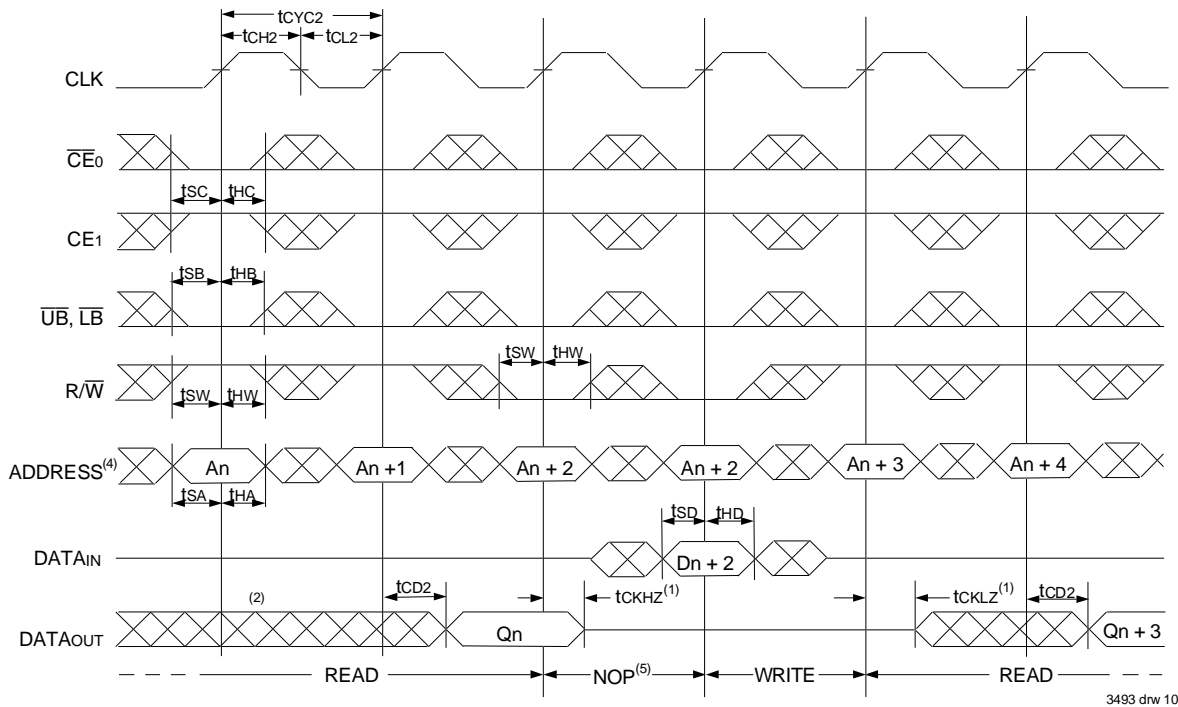


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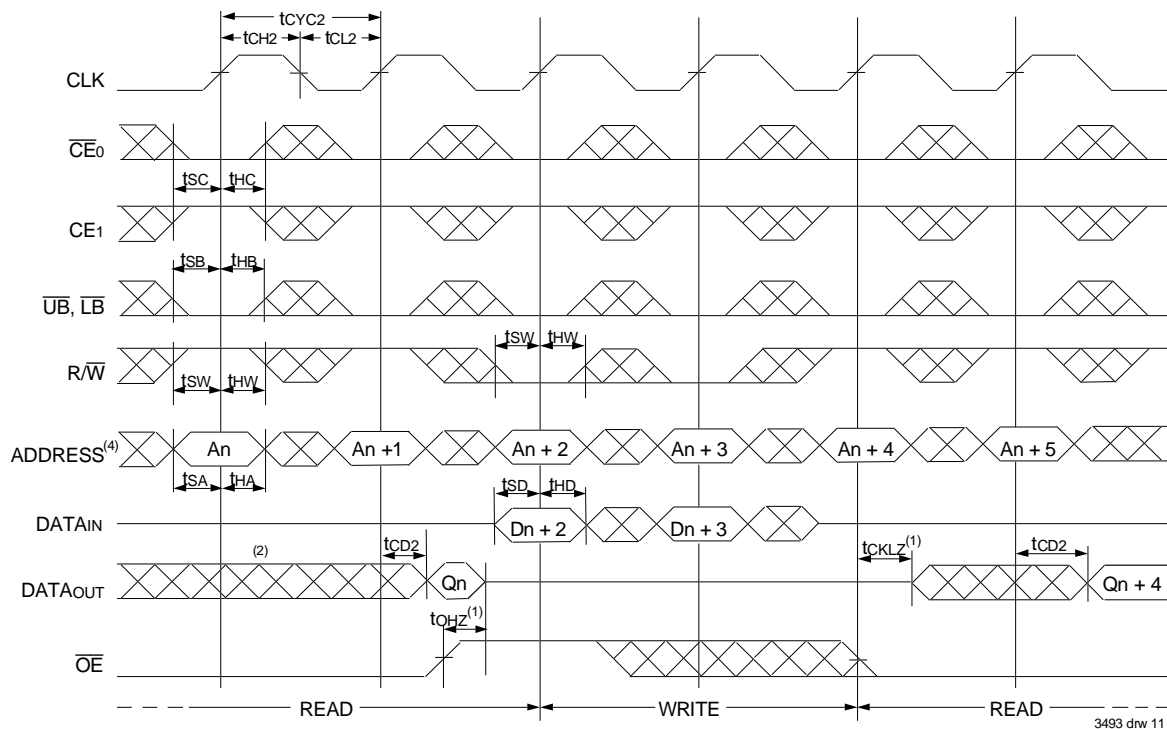
NOTES:

1. B1 Represents Device #1; B2 Represents Device #2. Each Device consists of one 709269 for this waveform, and are set up for depth expansion in this example. ADDRESS(B1) = ADDRESS(B2) in this situation.
2. \overline{UB} , \overline{LB} , \overline{OE} , and $\overline{ADS} = V_{IL}$; $CE_{1(B1)}$, $CE_{1(B2)}$ R/\overline{W} , \overline{CNTEN} , and $\overline{CNRST} = V_{IH}$.
3. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
4. \overline{CE}_0 , \overline{UB} , \overline{LB} , and $\overline{ADS} = V_{IL}$; CE_1 , \overline{CNTEN} , and $\overline{CNRST} = V_{IH}$.
5. $\overline{OE} = V_{IL}$ for the Right Port, which is being read from. $\overline{OE} = V_{IH}$ for the Left Port, which is being written to.
6. If $t_{CCS} \leq$ maximum specified, then data from right port READ is not valid until the maximum specified for t_{CWDD} . If $t_{CCS} >$ maximum specified, then data from right port READ is not valid until $t_{CCS} + t_{CD1}$. t_{CWDD} does not apply in this case.

Timing Waveform of Pipelined Read-to-Write-to-Read ($\overline{OE} = V_{IL}$)⁽³⁾



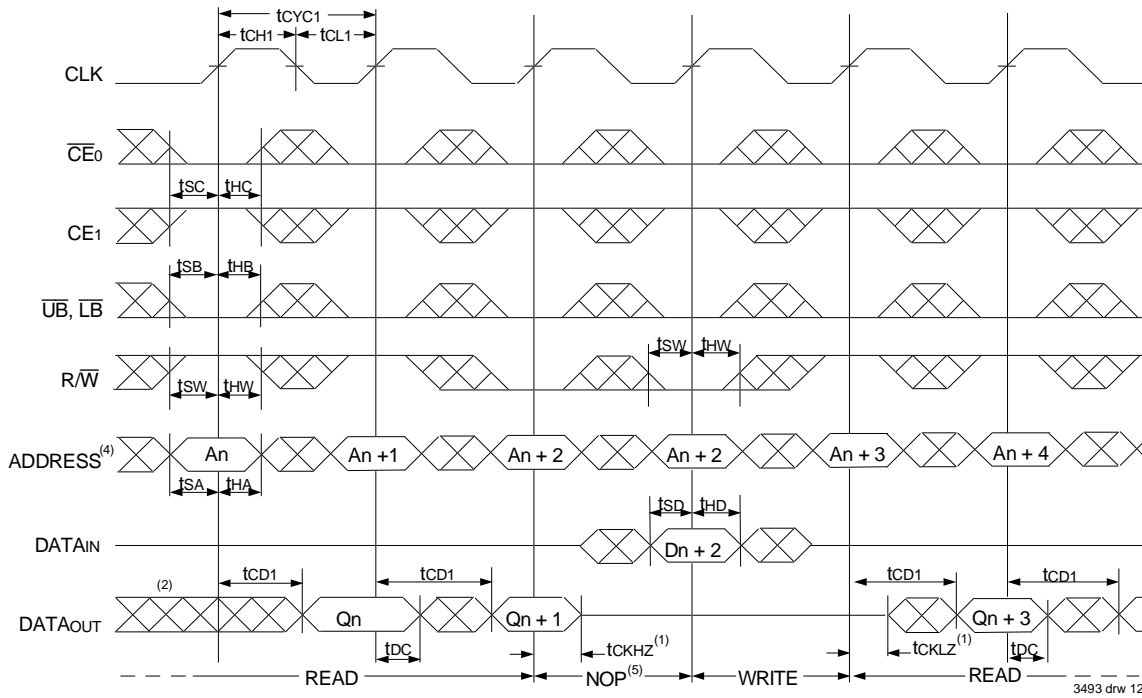
Timing Waveform of Pipelined Read-to-Write-to-Read (\overline{OE} Controlled)⁽³⁾



NOTES:

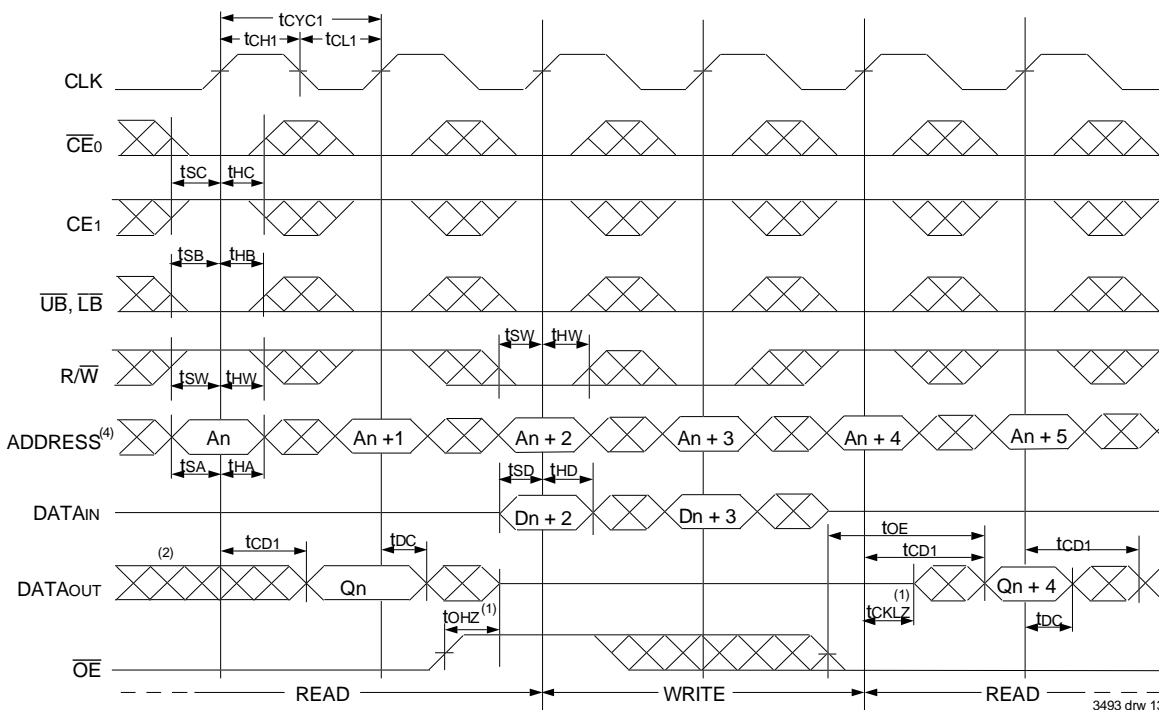
1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
3. $\overline{CE0}$, \overline{UB} , \overline{LB} , and $\overline{ADS} = V_{IL}$; $CE1$, \overline{CNTEN} , and $\overline{CNTRST} = V_{IH}$.
4. Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

Timing Waveform of Flow-through Read-to-Write-to-Read ($\overline{OE} = V_{IL}$)⁽³⁾



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Timing Waveform of Flow-through Read-to-Write-to-Read (\overline{OE} Controlled)⁽³⁾

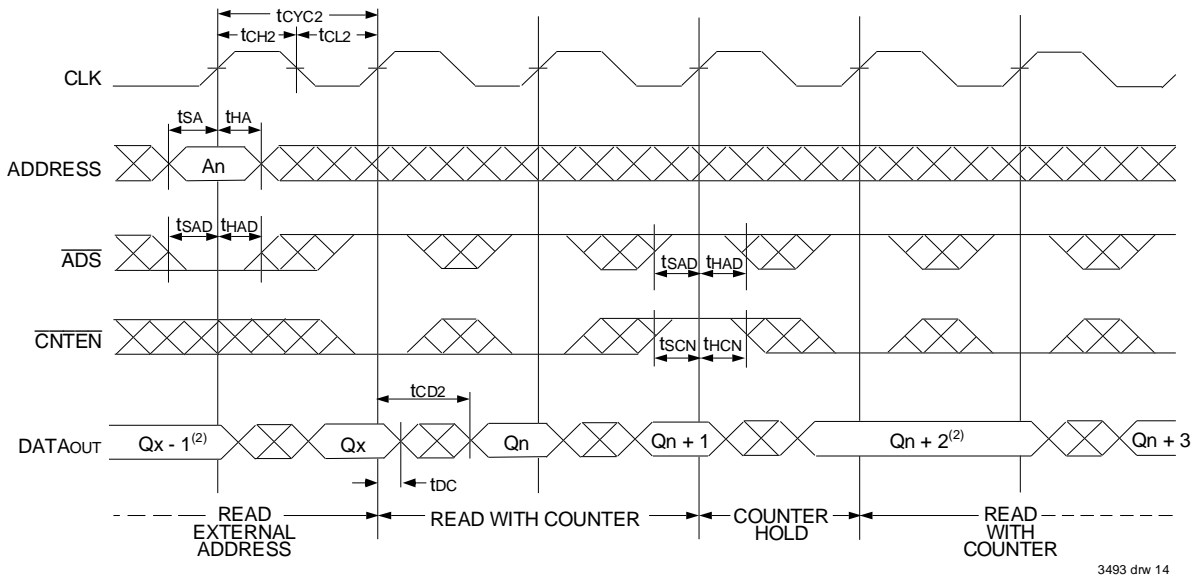


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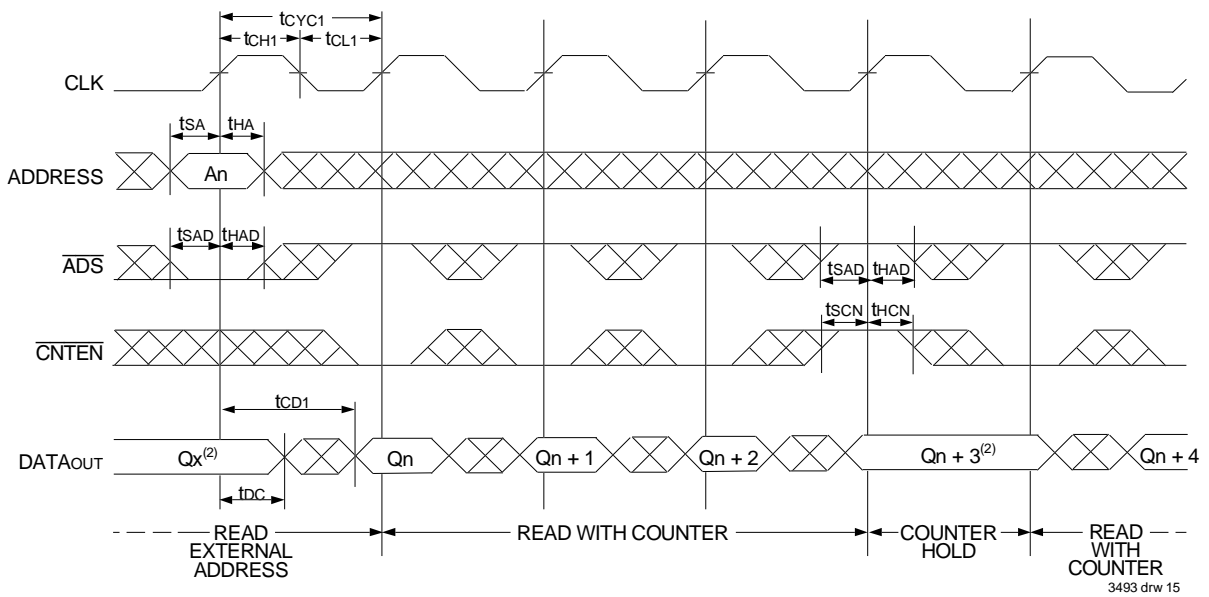
NOTES:

1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. Output state (High, Low, or High-impedance is determined by the previous cycle control signals.
3. \overline{CE}_0 , UB, LB, and ADS = V_{IL} ; CE1, CNTEN, and CNTRST = V_{IH} .
4. Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

Timing Waveform of Pipelined Read with Address Counter Advance⁽¹⁾



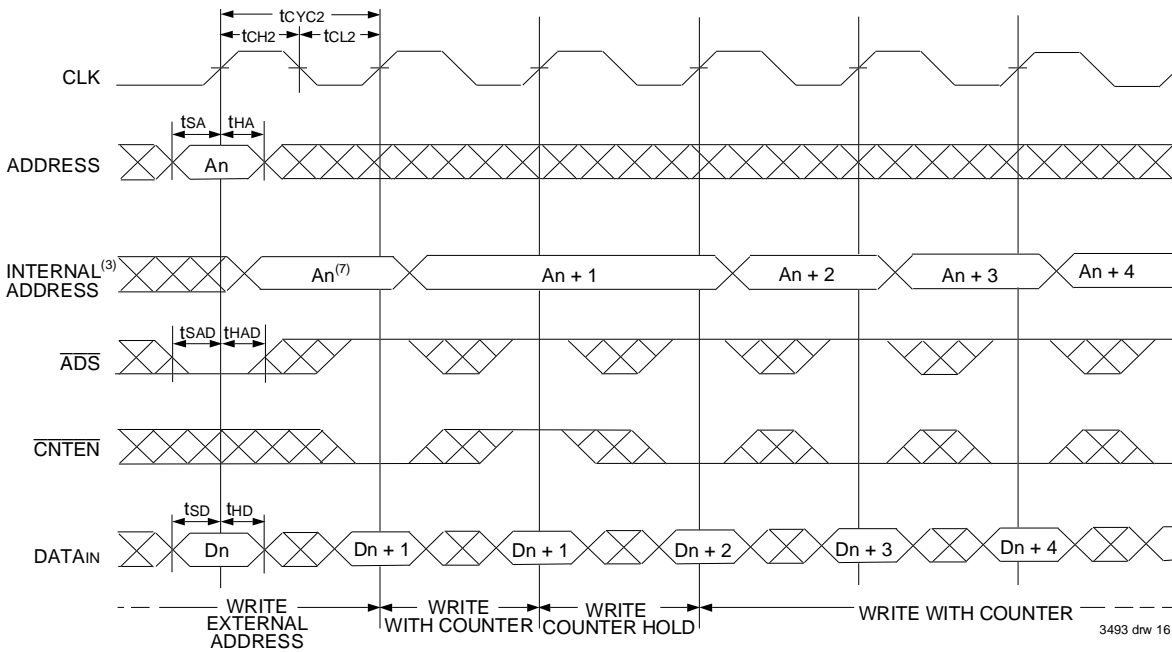
Timing Waveform of Flow-through Read with Address Counter Advance⁽¹⁾



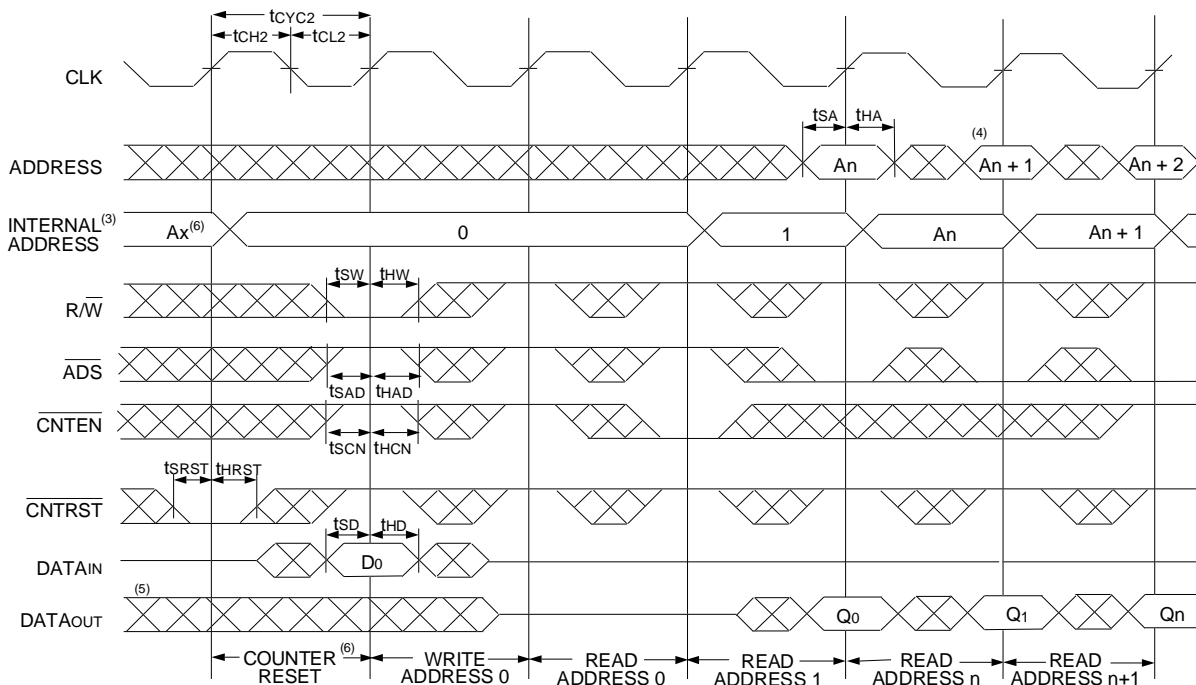
NOTES:

1. \overline{CE}_0 , \overline{OE} , \overline{UB} , and $\overline{LB} = V_{IL}$; CE_1 , $R\overline{W}$, and $\overline{CNTRST} = V_{IH}$.
2. If there is no address change via $\overline{ADS} = V_{IL}$ (loading a new address) or $\overline{CNTEN} = V_{IL}$ (advancing the address), i.e. $\overline{ADS} = V_{IH}$ and $\overline{CNTEN} = V_{IH}$, then the data output remains constant for subsequent clocks.

Timing Waveform of Write with Address Counter Advance (Flow-Through or Pipelined Outputs)⁽¹⁾



Timing Waveform of Counter Reset (Pipelined Outputs)⁽²⁾



NOTES:

- \overline{CE}_0 , \overline{UB} , \overline{LB} , and $\overline{R/W}$ = V_{IL} ; \overline{CE}_1 and \overline{CNTRST} = V_{IH} .
- \overline{CE}_0 , \overline{UB} , \overline{LB} = V_{IL} ; \overline{CE}_1 = V_{IH} .
- The "Internal Address" is equal to the "External Address" when $\overline{ADS} = V_{IL}$ and equals the counter output when $\overline{ADS} = V_{IH}$.
- Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
- Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
- No dead cycle exists during counter reset. A READ or WRITE cycle may be coincidental with the counter reset cycle. ADDR 0 will be accessed. Extra cycles are shown here simply for clarification.
- $\overline{CNTEN} = V_{IL}$ advances Internal Address from 'An' to 'An + 1'. The transition shown indicates the time required for the counter to advance. The 'An + 1' Address is written to during this cycle.

Functional Description

The IDT709269 provides a true synchronous Dual-Port Static RAM interface. Registered inputs provide minimal set-up and hold times on address, data, and all critical control inputs. All internal registers are clocked on the rising edge of the clock signal, however, the self-timed internal write pulse is independent of the LOW to HIGH transition of the clock signal.

An asynchronous output enable is provided to ease asynchronous bus interfacing. Counter enable inputs are also provided to stall the operation of the address counters for fast interleaved memory applications.

A HIGH on \overline{CE}_0 or a LOW on CE_1 for one clock cycle will power down the internal circuitry to reduce static power consumption. Multiple chip enables allow easier banking of multiple IDT709269's for depth expansion configurations. When the Pipelined output mode is enabled, two cycles are required with \overline{CE}_0 LOW and CE_1 HIGH to re-activate the outputs.

Depth and Width Expansion

The IDT709269 features dual chip enables (refer to Truth Table I) in order to facilitate rapid and simple depth expansion with no requirements for external logic. Figure 4 illustrates how to control the various chip enables in order to expand two devices in depth.

The 709269 can also be used in applications requiring expanded width, as indicated in Figure 4. Since the banks are allocated at the discretion of the user, the external controller can be set up to drive the input signals for the various devices as required to allow for 32-bit or wider applications.

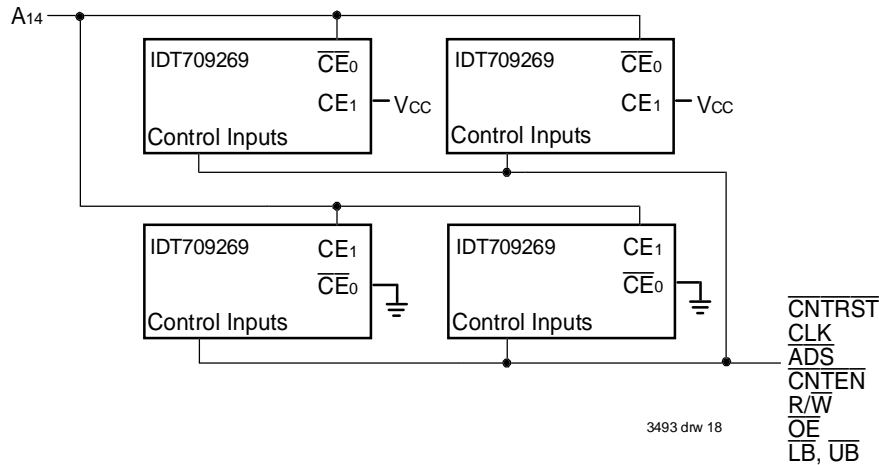


Figure 4. Depth and Width Expansion with IDT709269

Ordering Information

IDT	XXXXX	A	99	A	A	
	Device Type	Power	Speed	Package	Process/ Temperature Range	
						Blank (⁽¹⁾)
						Commercial (0°C to +70°C) Industrial (-40°C to +85°C)
						PF
						100-pin TQFP (PN100-1)
						9
						12
						15
						Commercial Only Commercial Only Commercial Only
						} Speed in nanoseconds
						S
						L
						Standard Power Low Power
						709269
						256K (16K x 16-Bit) Synchronous Dual-Port RAM

3493 drw 19

NOTE:

1. Industrial temperature range is available.
 For specific speeds, packages and powers contact your sales office.

Preliminary Datasheet:

"PRELIMINARY" datasheets contain descriptions for products that are in early release.

Datasheet Document History

- 1/12/99: Initiated datasheet document history
 Converted to new format
 Cosmetic and typographical corrections
 Added additional notes to pin configurations
 Page 14 Added Depth & Width Expansion note
- 6/7/99: Changed drawing format
 Page 4 Deleted note 6 for Table II
- 4/17/00: Replaced IDT logo
 Added FT/PIPE to left port.
 Changed ±200mV to 0mV in notes



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